APPLICATION OF I_{DDT} TEST IN SRAM ARRAYS TOWARDS EFFICIENT DETECTION OF WEAK OPENS

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Abstract. This paper deals with the dynamic supply current testing (I_{DDT}) of SRAM cells and arrays. Additionally, an I_{DDT} current sensor and used current sensing method are presented and explained as well. The efficiency of the proposed test in unveiling weak open defects is demonstrated through simulations carried out on a 64 bit SRAM array designed in a CMOS 90 nm technology. Also the dependence of the efficiency on the cell ratio of the SRAM core cell is evaluated.

Keywords. Dynamic supply current test, I_{DDT}, current sensor, SRAM array, 6-transistor SRAM cell, memory test, weak opens, defect coverage.

1 Introduction

According to the International Roadmap for Semiconductors (ITRS), memories are occupying more than 90 % of the total SoC area [1]. Thus, memory test represents a serious issue, where the reliability of memories has a deep impact on the overall SoC yield. Since SRAMs are the most often used embedded memories that is why the testing of these memories is in the center of attention recently.

The most straightforward tests are conventional logic tests, which in first place are meant to test the logic function of a given circuit. In the case of SRAMs, the main function is to store a logic value. Though, it differs from logic circuits, which are processing logic input signals. The input is basically a sequence of write operations. To see the correct result, one must provide read operations. This, and the ever growing storage capacity of SRAMs causes that the logic test is becoming ineffectively long and quite difficult. In practice, the logic test is realized by march-based tests, which are meant to test each cell and additional circuitry (addressing decoders, logic buffers, etc.) as well [2].

However, there are defects, which do not cause malfunction of the circuit even though they are present in the circuit. Instead, these defects might be the source of reliability issues appearing within time. Thus, such defects might escape conventional logic test methods. A very actual problem is the presence of open defects, and especially hard detectable weak open defects [1]. Particularly, in nanometer scaled technologies where copper metallization is used, open defects have become a serious problem [3].

Taking all the issues mentioned above into account, alternative test methods used to augment the conventional test have to be developed. These techniques are based on the measurement and monitoring of some circuit's parameters, such as temperature or the current consumption. The dynamic supply current test method (I_{DDT} testing), which is meant to unveil resistive open defects, is based on the monitoring of the dynamic current consumption of the tested circuit.

1.1 Research objectives

Based on the state-of-the-art analysis as well as known needs in the respective test field, the following research objective for the PhD thesis have been defined:

- Investigation of I_{DDT} testing as a proper augmenting test method to extensive voltage-based tests in SRAMs, the analysis of its efficiency.
- Evaluation of feasibility/effectiveness of standard March tests for I_{DDT} testing of SRAMs and/or the development of a dedicated TP generator for the designed I_{DDT} test.
- Analysis of I_{DDT} waveform parameters versus fault coverage, the definition of the most efficient parameter to be sensed, and investigation of on-chip versus off-chip measurement/processing.
- Design of I_{DDT} test hardware for SRAM array and its implementation in deep-submicron technology with respect to area overhead and power consumption.
- Implementation of the proposed test hardware taking into account "Design-for-I_{DDT}-Testability".
- Evaluation of the proposed approach as well as the developed hardware on an experimental SRAM array chip designed in submicron technology.

2 Open defects

Open defects can be classified based on the resistance value they are representing. The most straightforward classification is that open defects with the resistance values higher than 10 MΩ are considered to be hard opens, and opens with the resistance values under 10 MΩ are weak open defects [1]. On the other hand, weak opens are generally difficult to detect, while hard opens usually cause simple stuck-at faults.

This also means that hard opens are easier to unveil with simple march tests, while weak opens cause faults that are more difficult to model and thus, detect. That is why the main focus of this paper is on unveiling weak open defects.

2.1 Logic tests for open defects

One of the results of open defects present in a circuit is, that they can cause delay along a given path. A circuit is considered to have a delay fault, if the output fails to reach the right value within a certain time [4]. However, in the case of SRAMs, the only way to check the right output value is to read out the stored values, what makes the test longer and more complicated.

Open defects may cause random variations in the timing of SRAM memories. Delay caused by open defects can be mapped into several dynamic and static fault models for SRAMs. These are Read Destructive Faults (RDF), Deceptive Read Destructive Fault (DRDF), Incorrect Read Fault (IRF) and Transition Fault (TF). All of these faults are related to open defects present in different places along the SRAM core cell and usually, their detection requires different types of march tests [5]. However, several rather universal march test solutions have been presented so far, e. g. in [5, 6, 7].

The efficiency of the abovementioned march test solutions is moderate or good. Some methods effectively unveil open defects with the resistance values of several 10 kΩ already, while other methods can only detect open defects of the resistance values of several MΩ. Nevertheless, several factors were neglected in those approaches, like the Cell Ratio (ratio of the dimensions of the pull-down transistor to the access transistor), or the Pull-up ratio (ratio of the dimensions of the pull-up transistor to the access transistor) of the core cell [2].

The main advantage of march test solutions is that some resistive-open defects can be unveiled from quite low resistance values, and the march test for these defect types could be performed as an at-speed test. On the other hand, some of the open defects cannot be unveiled from low resistance values but rather high values (several MΩ), and the march test requires several read and write operations.

2.2 I_{DDT} test

The I_{DDT} test represents an alternative test method to logic tests. It has a good ability in unveiling resistive-open defects, because open defects affect the dynamic behavior of a logic circuit the most. Also it is related to delay faults, because delay faults can cause edge rate degradation as well, where the rise and fall times are influenced [4]. In [8], a mathematical approximation was constructed for the dynamic current of an inverter, from which it is straightforward that the rise time and fall time of the digital voltage affects also the dynamic supply current.

Detailed discussion on I_{DDT} test in general is presented in [9, 10, 11]. One of the main advantages of I_{DDT} test is the simplicity of test generation, where only two write operations are needed for testing each cell. This makes the test faster but on the other hand, at-speed test could represent a problem in the case of more complex additional circuitry.

3 I_{DDT} based current sensor

The general concept of the current sensing circuitry is depicted in Fig. 1a. It consists of three basic building blocks. The first block is “Current sensing and conversion to voltage”, where the CUT represents a SRAM cell array. The voltage drop variation, caused by the dynamic current consumption of the SRAM array, across a serially connected PMOS transistor is sensed. The second block is “Voltage Amplification” circuitry, by which the voltage drop is amplified. The third block is the “Evaluating circuitry with digital output”, where the peak of the amplified voltage is sensed by a peak detector. Finally, the value of the voltage peak is compared to two voltage thresholds. Depending on the output value of the voltage comparator, a simple logic circuit (e.g. XOR) generates a single output digital signal indicating the state (defective or defect-free) of the tested circuit.

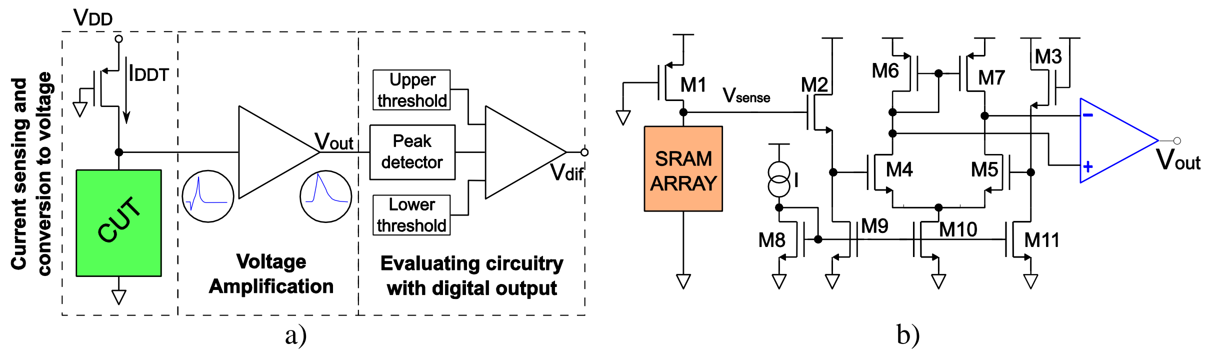

Figure 1: a) Current sensor concept, b) Peak amplifier concept

The detailed topology of the first two blocks from Fig. 1a, is depicted in Fig. 1b. The design was done in a 90 nm CMOS technology, which represents many challenges for analog design, where transistors have rather low gain factors, and the supply voltage used was 1.2 V.

Sensing of the dynamic current was based on voltage to current conversion. Because resistors in the given technology are of unacceptably large dimensions, a PMOS transistor (M1 in Fig. 1b) with a grounded gate was used instead. The channel length of the transistor was kept minimal, while the channel width was set to a considerably higher value. The main factors behind the choice of the width to length ratio of M1 were the voltage drop, which should not affect the SRAM power supply voltage but in the meantime, shall assure a voltage drop big enough to be sensed and amplified, and the sensing element area overhead.

For the purpose of the sensed voltage amplification, a slightly modified differential amplifier together with an operational amplifier was used. The differential amplifier consists of NMOS differential pair M4-M5, which are faster and have higher gain factor than PMOS transistor

alternative, and an active load created by a slightly modified PMOS cascode current mirror (M7-M10). M6 is used as a resistor. This load has more precise mirroring compared to a simple current mirror, and also has higher output impedance, which assures higher voltage gain. The second and third amplifying stage is assured by a conventional operational amplifier.

The input of the amplifier is separated from the voltage source (drain of M1 - V_{sense}) with an NMOS voltage follower M2. This assures better DC condition at the input of the differential amplifier. In a static state, the voltage drop across M1 is nearly zero. That means that the voltage at the drain of M1 is equal to the power supply of 1.2 V. The voltage follower is fed with the same current as the differential amplifier and voltage follower composed of M3. M3 has the same dimensions as M2, and is used to create the same DC condition at the other input of the differential amplifier. By shorting its gate to the power rail, and by having size of M12 and M14 equal, the DC conditions at the inputs of the differential amplifier are equal too.

3.1 Processing the charge involved in the current peak

In [9, 10, 11], the parameters of the I_{DDT} waveform were already presented. In this section, the method of conversion of one of the parameters, namely the charge provided by the dynamic current waveform, to a voltage peak value will be presented.

In Fig. 2a, the conversion of the I_{DDT} waveform to an output voltage is presented. It can be seen that the voltage at the drain of M1 (dotted line) copies the I_{DDT} waveform (solid line) rather well, and the final output voltage (V_{out} from Fig. 1b – dashed line) also has the characteristics of the dynamic current waveform.

In Fig. 2b, the voltage on gate (solid line) and voltage at the drain (dotted line) of M4 are depicted. From Fig. 1a and Fig. 1b it can be observed that the voltage on gate of M4 copies the voltage at V_{sense}, and the voltage at drain of M4 copies the gate voltage of M4. In Fig. 2c, the current waveform I_4 (dotted line) and the output voltage of the amplifying circuitry V_{dif} (solid line) is depicted.

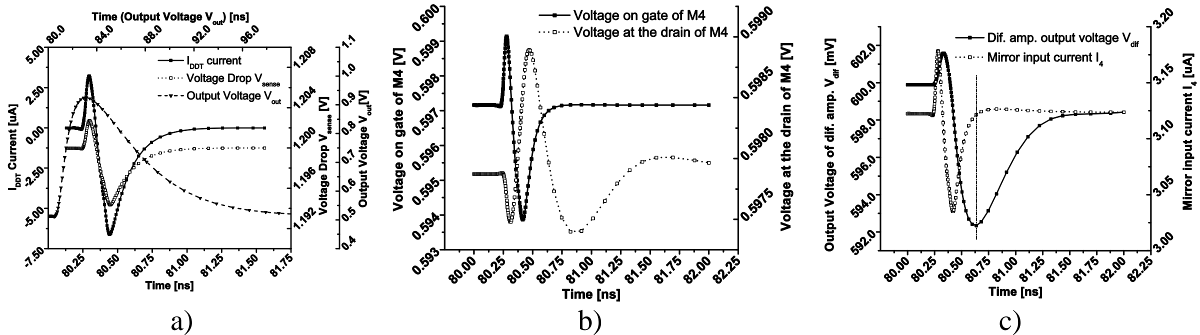

Figure 2: Voltage and current waveforms at given nodes of the sensing circuit

One can observe that the current waveform I_4 still has the characteristics of the original I_{DDT} waveform, both in shape and in time too. However, the dynamic current I_4 compared to the I_{DDT} current is considerably smaller. Let us assume that when the circuit is in a static state, I_4 is in static state too. Then when the I_{DDT} waveform appears, I_4 gets in a dynamic state too. From the function of the basic current mirror it is obvious, that the output current is controlled by modulating the voltage at the gate of the output transistor of the current mirror (in this case M8 and M10). From the physical point of view, every time the input current changes, it first has to charge or discharge the gate capacitances of the current mirror (in this case M7-M10) to the given value of voltage to reach the desired output current. In the case of the current sensor from Fig. 1b, the gate capacitances of M7-M10 act like an integrator, and I_4 basically charges this capacitance. Thus, the output voltage V_{dif} keeps

rising till the current settles again in a static state. This moment is depicted with the vertical line (Fig. 3c). From this moment on, the capacity of the mirror transistors is discharged by the static part of I_4.

It can be also observed that I_4 copies really well the I_{DDT} waveform, so there is a presumption that it will contain the same information about defects present in the circuit as the I_{DDT} waveform. This way, basically the charge carried by the current pulse I_{DDT} is converted to the output voltage peak. The efficiencies of the single I_{DDT} waveform and then the output voltage V_{dif} of the amplifying circuitry is compared and evaluated in the next section, where also the importance of the presented method will be explained.

4 Efficiency of the proposed method

The efficiency of the proposed I_{DDT} test method on a theoretical basis, where no sensing circuitry was used in simulations performed on a 64-bit SRAM circuit in a 90 nm CMOS technology is shown in Tab. 1. The methods of simulations and the calculation of efficiencies are described in [9, 10, 11], where certain parameters of the dynamic current waveform were analyzed. These parameters that are common for both current and voltage waveforms are the peak value, the width, the average value, and the time of the peak (usually the one with the least information about defects present). The simulations were performed in order to gain data about the efficiency of this test method for different SRAM cell ratios (1, 1.5, 2, and 2.5). The pull-up ratio was kept one, while the dimensions were set to minimum.

The open defects were modeled by the parallel combination of a single resistor and a capacitor. The value of the resistors was swept from 10 kΩ to 1 MΩ in three steps, while the capacitor has a low, almost negligible value.

Efficiency of the dynamic output voltage V_{DDT} at node V_{dif} is shown also in Tab. 1. For the purpose of evaluation of the voltage waveform similar parameters were stated to those of the current waveform. When compared to the results of I_{DDT}, one can see that the efficiencies are similar. Though much worse for lower values of opens, but comparable at higher values of opens.

Table 1: Efficiency of sensing and evaluating I_{DDT} and V_{DDT}

R [Ω]	CR							
	1	1.5	2	2.5	1	1.5	2	2.5
	Efficiency of I_{DDT} [%]				Efficiency of V_{DDT} [%]			
10K	21.7	34.8	47.8	39.1	8.7	4.3	17.4	26.1
100K	87	87	82.6	87	82.6	78.2	82.6	82.6
1M	100	100	100	100	100	100	100	100

Another interesting issue to be discussed is the efficiency of the parameters of the I_{DDT} current waveform and the V_{DDT} waveform. The only V_{DDT} waveform parameter that differs from that of the current waveform is the waveform integral because in the case of the current waveform, the integral is the charge provided by the current. For the voltage waveform the integral was calculated. In Tab. 2, the efficiency of the parameters of the two waveforms is presented.

Table 2: Efficiency of the parameters of the I_{DDT} and V_{DDT} waveforms

Parameter	Efficiency of I_{DDT}			Efficiency of V_{DDT}		
	R[Ω]					
	10 k	*100 k*	*1 M*	*10 k*	*100 k*	*1 M*
Width	9 %	69.6 %	100 %	0 %	34.8 %	65 %
Average	4.3 %	78.3 %	100 %	4.3 %	78.3 %	100 %
Charge/Integ.	21.7 %	87 %	100 %	0 %	52.2 %	100 %
Peak Value	13 %	52.2 %	74 %	4.3 %	78.3 %	100 %

From Tab. 2, one can observe that the most effective parameter of I_{DDT} is the charge provided by the dynamic current (integral of the dynamic current waveform), while the most effective parameter of the voltage waveform is the peak value and average value.

5 Conclusion

In our work, the efficiency and feasibility of the dynamic supply current test in covering weak open defects present in SRAM arrays was investigated. Firstly, the march test solution for open defects was presented, and its advantages and disadvantages were discussed. After that a concept of the I_{DDT} test hardware was presented, where the sensing and amplifying blocks were realized in a 90 nm CMOS technology. The amplifying stage is based on the conversion of the charge provided by the current waveform to a voltage peak value.

Interesting results were achieved, which supports the feasibility expectations for the proposed sensor. The efficiency of both I_{DDT} as well as V_{DDT} is presented, and the efficiency of the parameters of the dynamic current and dynamic voltage waveform was evaluated too. The most efficient parameter of I_{DDT} is the charge included in the current peak, while the most efficient parameter of the dynamic voltage is the peak value.

It was also shown that the test vectors consist of two write operations of the opposite direction. This also means that basically, all the march tests, which contain at least two write operations of the opposite direction and are performed anyway on SRAMs could be enough to test the SRAM array for the presence of resistive-opens. Thus, one of the research objectives seems to have an easier solution.

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